

## AMENDMENTS TO THE CLAIMS

32. (New) A processor comprising:

a first clock circuit to clock a first functional unit while the first functional unit is not being tested;

a second clock circuit to clock a second functional unit independently of the first clock circuit while the second functional unit is being tested.

33. (New) The processor of claim 32 wherein the second clock circuit comprises a cluster test controller, a unit test controller, and a local test clock controller.

34. (New) The processor of claim 33 wherein the functional unit comprises a plurality of functional units.

35. (New) The processor of claim 34 further comprising a third clock circuit to at least partially control the plurality of functional units independently of the functional clock circuit.

36. (New) The processor of claim 35 wherein the third clock circuit comprises a master clock generation unit and a slave clock generation unit.

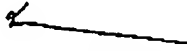
37. (New) The processor of claim 36 wherein the first clock circuit is to couple a functional clock signal to the first and second functional units during normal operation of the first and second functional units.
38. (New) The processor of claim 37 wherein the second clock circuit is to couple a functional clock signal to the first and second functional units during testing of the first and second functional units.

If there are additional fees due, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

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